REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	5/14/04	Reprint

4. TITLE AND SUBTITLE

A Compensation-Based Optimization Methodology for Gain-Boosted OPAMP

5. FUNDING NUMBERS

N00014-94-1-0931

6. AUTHOR(S)

Jie Yuan and Nabil Farhat

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Nabil H. Farhat
University of Pennsylvania
ESE Department
200 South 33rd Street
Philadelphia, PA 19104-6390

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Defense Technical Information Center
8725 John J. Kingman Road, Ste. 0944
Fort Belvoir, VA 22060-6218

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT

DISTRIBUTION STATEMENT A
Approved for Public Release
Distribution Unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

A gain-boosted OPAMP design methodology is presented. The methodology provides a systematic way of gain-boosted OPAMP optimization in terms of AC response and settling performance. The evolution of the major poles and zeros of the gain-boosted OPAMP is studied, which reveals the rationale behind our optimization effort. A sample OPAMP was implemented in 0.6 μm CMOS technology. It achieves a DC gain of 88dB, a bandwidth of 725MHz with 49° phase margin and a 0.1 settling time of 4.5ns. The sample/hold front-end of a 12-bit 50MSample/s ADC was implemented with this OPAMP. It achieves an SNR of 78dB for an 8.1MHz input signal.

14. SUBJECT TERMS	15. NUMBER OF PAGES
	4
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	

IEEE Int. Symp. on Circuits and Systems (ISCAS '04)

A COMPENSATION-BASED OPTIMIZATION METHODOLOGY FOR GAIN-BOOSTED OPAMP

Jie Yuan, Nabil Farhat

Electrical and System Engineering Department
University of Pennsylvania

ABSTRACT

A gain-boosted OPAMP design methodology is presented. The methodology provides a systematic way of gain-boosted OPAMP optimization in terms of AC response and settling performance. The evolution of the major poles and zeros of the gain-boosted OPAMP is studied, which reveals the rationale behind our optimization effort. A sample OPAMP was implemented in 0.6 μm CMOS technology. It achieves a DC gain of 88dB, a bandwidth of 725MHz with 49° phase margin and a 0.1% settling time of 4.5ns. The sample/hold front-end of a 12-bit 50MSample/s ADC was implemented with this OPAMP. It achieves an SNR of 78dB for an 8.1MHz input signal.

1. INTRODUCTION

The operational amplifier is the most fundamental component in CMOS analog design. It is the critical component that, in most cases, is responsible for the performance of switch-capacitor circuits. In recent years, considerable effort has been made to design CMOS ADCs with higher sampling rates and better resolution. One of the essential tasks in all these efforts is to provide a better performance OPAMP, with higher gain, higher bandwidth, and faster settling time.

High-speed OPAMPs use only one stage to reduce the parasitics. Telescopic OPAMPs and folded-cascode OPAMPs are majorly used[1]. The gain boost technique proposed in [2] is normally used to achieve high gain by exploiting the principle of the regulated-cascode stage[3]. However, the existence of a doublet can unfavorably affect the settling performance of the gain-boosted OPAMP[2],[4]. The effort of pushing up the doublet can raise stability problem. As we will show later in our simulation, the complex conjugate pole pair reported in [5] and [6] will eventually push the system into instability. In this paper, we offer a compensation-based gain-boosted structure and an optimization methodology based on this structure that can optimize the design between the doublet and the stability issues.

This research was supported by the Office of Naval Research under grant No. N00014-94-1-0931 and by an Army Research Office MURI grant Prime DAAD 19-01-1-0603 via Georgia Institute of Technology subcontract E-18-677-64.

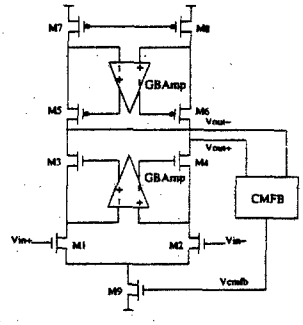

Fig. 1. Telescopic Gain-boosted OPAMP Structure

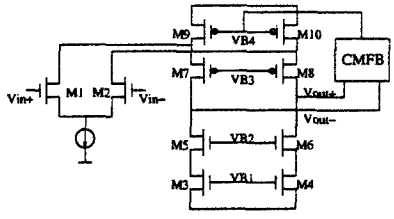

Fig. 2. The gain boost OPAMP circuit

2. THE GAIN BOOST TECHNIQUE

The gain-boosted OPAMP employs two amplifiers: the main OPAMP and the gain boost OPAMP (GBAmp). In Fig. 1, a telescopic gain-boosted OPAMP is given. the DC gain of the gain-boosted OPAMP would be

$$A_{DC} \approx \frac{1}{2}\frac{g_{m1}g_{m3}}{g_{ds1}g_{ds3}}A_{DCgb} \qquad (1)$$

Hence, the ideal effect of the GBAmp is to improve the DC gain by A_{DCgb} times. At the same time, it increases the output impedance by A_{DCgb} times so as to push down the dominant pole at the OPAMP's output node by A_{DCgb}, which leaves the high-frequency performance of the main OPAMP unchanged.

However, the characteristics of the GBAmp can potentially raise two significant problems for the settling performance of the OPAMP. There exists a doublet around the unity-gain frequency of GBAmp (ω_{ugb})[2]. Although the doublet might not be easily observed on the OPAMP's AC charts, it can greatly extend the settling process[4]. A common solution is to increase ω_{ugb} so as to push the doublet up to a higher frequency.

When the doublet is pushed high enough, the system is also susceptible to instability. As the doublet is pushed near the nondominant pole of the main OPAMP (ω_{ndmain}), [5] and [6] reported the generation of a pair of complex conjugate poles. The attempt to push this pair of poles to a higher place would reduce the phase margin of the circuit. Our simulation results, in later sections, reveal the dynamics of the major pole-zero development of the OPAMP. It verifies the existence of the pole pair. It also shows the existance of an optimal point in terms of the OPAMP's settling performance. Beyond this optimal point, the OPAMP starts to become unstable.

As a result, the design of the GBAmp needs to include an optimization process to balance the effort of reducing the doublet and the effort of keeping the system stable. A small compensation capacitance of several hundred femto farads is used for the GBAmp to manage the optimization process.

3. IMPLEMENTATION

The circuit is designed in a $0.6\mu m$ CMOS process. The supply voltage is 5V. A telescopic gain-boosted OPAMP in Fig. 1, referred to as OPAMP1, is designed below. Folded-cascode OPAMPs are used for GBAmps as shown in Fig. 2. We notice that the GBAmp will always have a smaller bandwidth than the main OPAMP because of the smaller biasing current with power consumption constraints. As given in [2],as long as $\omega_{ugb} < \omega_{ndmain}$, OPAMP1 will be stable. Therefore, OPAMP1 can always be kept stable with small compensation. However, GBAmp's phase margin can always be traded in for bandwidth to push up the doublet, which is partly the reason for the conflicts between the doublet problem and the stability problem. Also, considering the high gain that GBAmp needs to achieve, the small gate capacitances of M3-M6 in Fig. 1 are almost always not enough to provide a sufficient phase margin, which makes the small compensation capacitances necessary. The final bench test is a sample/hold front end for a 12-bits, 50MHz ADC, as shown in Fig. 3. The signal swing is -2V – +2V.

4. DESIGN METHODOLOGY AND SIMULATION RESULTS

As we discussed in Sec. 2, ideally the gain boost technique decouples the constraints on the OPAMP's gain and bandwidth, which enables us to adopt a three-step design methodology.

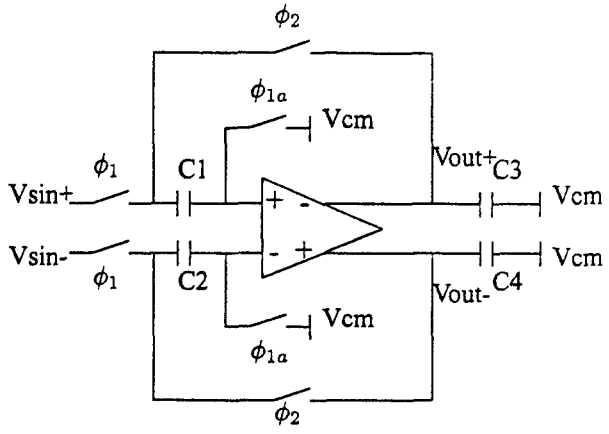

Fig. 3. The Sample/Hold Front End

4.1. Main OPAMP Design

The high frequency performance of OPAMP1 is determined by the main OPAMP, as we previously discussed. Therefore, the design goal in this phase is to achieve the specified unity gain bandwidth (Ω_u) within the specified power consumption.

The problem of obtaining the maximum unity gain bandwidth at a specified phase margin Φ_m with a given current has just one solution. The idea is to use the minimal transistor (W/L) set to reduce parasitics. We use the algorithm below to find this solution.

Algorithm 1 *: Main OPAMP Design*

INPUT : bandwidth spec Ω_u, bandwidth cushion Ω_{cu}, phase margin spec Φ_m, phase margin cushion Φ_{cu}, maximum current I_{max}, biasing region of each transistor BR, $(W/L)_1$ and $(W/L)_2$ update rule $UR1$, (W/L) update rule for the other transistors $UR2$, external bias voltage and load ENV;

OUTPUT : a (W/L) solution and a current I that meets the specs, or a failure signal.

0. pick a current $I < I_{max}$;
1. **if** $I > I_{max}$, **return** failed;
2. pick a "reasonable" (W/L) set $(W/L)_{set}$;
3. $[\omega_u, \phi_m] := ACanalysis((W/L)_{set}, I, ENV)$;
4. **if** any transistor $\notin BR$, **goto** 5;
   else if $\omega_u > \Omega_u$ and $\phi_m > \Phi_u$; successful; **goto** 5;
   else if $\omega_u < \Omega_u$; $UR1((W/L)_{1-2}, +)$; **goto** 3;
   else if $\omega_u > (\Omega_u + \Omega_{cu})$; $UR1((W/L)_{1-2}, -)$; **goto** 3;
   else if $\phi_m < \Phi_m$, $UR2((W/L)_{3-8}, -)$; **goto** 3;
5. **if** no solution results, $I := I + \Delta I$; **goto** 1;

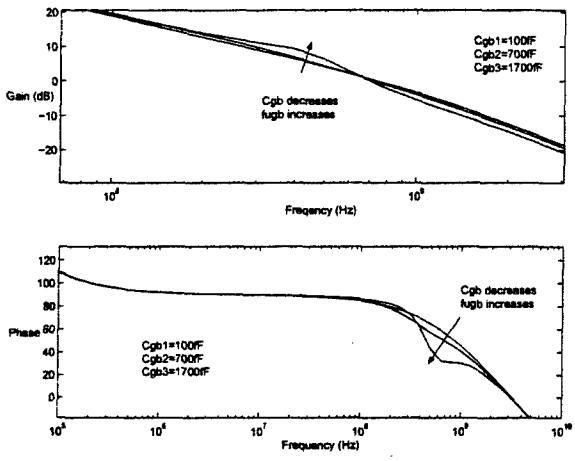

Fig. 4. AC performances with different GBAmp compensations

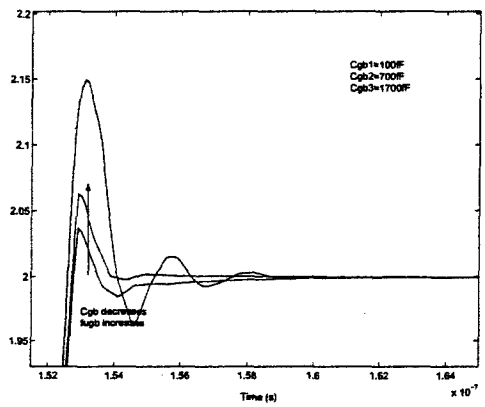

Fig. 5. Settling performances with different GBAmp compensations

else return successful.

If the algorithm fails to generate a solution, the current design specifications would be too stringent for the current CMOS process. Therefore a more advanced process is required, the power specification should be increased, or the BR is to be reduced with the tradeoff of a smaller output swing. If the specifications are loose, the solution can then be optimized according to different rules, such as power to be minimized or bandwidth to be maximized.

For OPAMP1, the designed main OPAMP achieves a unity-gain bandwidth of 770MHz with a phase margin of 58°. It requires a bias current $I_m = 4$mA. The resulting gain is $A_{DCmain} = 45$dB.

4.2. GBAmp AC Design

The design goal in this phase is to have a GBAmp achieving the specified DC gain and the best phase chart in terms of nondominant poles under a specified bias current. The gain of the GBAmp in Fig. 2 can be increased either by increasing $(W/L)_{1,2}$ to have higher g_m or by increasing the size of M3-M10 to achieve a higher output impedance. Either approach will,however, deteriorate the phase chart. So, with the power constrained, the GBAmp design problem becomes a two-dimensional optimization problem. Fortunately, the two variables in this problem, $(W/L)_{1,2}$ and the size of M3-M10, have discrete values within a finite practical space. All meaningful combinations can be checked through with computers to find the optimal solution. In our design process, only 10 "meaningful" (W/L) combinations have been tried out. Algorithm below is used to reach the optimal solution.

Algorithm 2 *: GBAmp Design*

INPUT : gain spec A_{DCgb}, gain spec cushion A_{DCcugb}, maximal allowed bias current I_{maxgb}, biasing region of each transistor BR, $(W/L)_{1-2}$ update rule $UR1$, (W/L) update rule for M3-M10 $UR2$, external bias voltage and load ENV, the meaningful (W/L) space Γ;

OUTPUT : a configuration with gain spec met and best phase chart within the maximal current.

0. $L := L_{min}, \Omega_{ndgb} := 0$;
1. Pick a "reasonable" (W/L) set;
2. $OPanalysis((W/L)_{set}, I_{max}, ENV)$;
3. **if** all the transistor $\in BR$
   then $UR2((W/L)_{3-8}, -)$;
   goto 2;
   else recover the previous $(W/L)_{3-8}$;
4. $[a_{dc}, \omega_{ndgb}] := ACanalysis((W/L)_{set}, I_{max}, ENV)$;
5. **if** $a_{dc} < A_{DCgb}$
   then $UR1((W/L)_{1-2}, +)$;
   goto 4;
   else if $a_{dc} > (A_{DCgb} + ADCcugb)$
   then $UR1((W/L)_{1-2}, -)$;
   goto 4;
6. **if** $(W/L)_{1-10} \notin \Gamma$, **goto** 7;
   else if $\omega_{ndgb} > \Omega_{ndgb}$
   then $\Omega_{ndgb} := \omega_{ndgb}$;
   $UR2((W/L)_{3-8}, +)$;
   goto 4;
7. **if** the L space has not been exhausted yet
   then $L := L + \Delta L$;
   goto 1;
   else end.

4.3. Settling Performance Optimization

The design goal of this phase is to determine the compensation that enables OPAMP1 to achieve the fastest settling

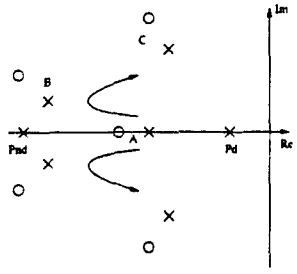

Fig. 6. Pole-zero evolution of OPAMP1 with ω_{ugb}

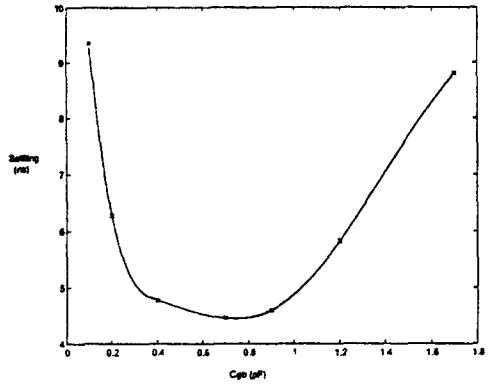

Fig. 7. Relationship between settling time and C_{cgb}

time. In Fig. 4, the AC performance of the designed OPAMP1 is plotted against different GBAmp compensations. Because different GBAmp compensation results in different ω_{ugb}, Fig. 4 is also the AC performance under different unity-gain bandwidths of GBAmp. The corresponding transient performance is shown in Fig 5.

Using Matlab simulation, the major pole-zero evolution of OPAMP1 can be inferred, as shown in Fig. 6. At large compensation, or when ω_{ugb} is as low as at position A, the doublet can be seen moving up in frequency as ω_{ugb} increases. In this phase, the settling time reduces as ω_{ugb} increases. When the doublet moves to a higher frequency, a pair of complex conjugate poles is generated, as reported in [5] and [6]. Further increasing ω_{ugb} can push the complex conjugate pole pair up along the real axis, which continues reducing OPAMP1's settling time. However, it also pushes the pair away from the real axis, which gives way to oscillation in the time domain. Beyond some point, such as B, the pair starts to move back along the real axis while it continues moving away from the real axis. In this phase, the envelope settling time starts to increase instead, as does the oscillation frequency for the transient output. The dampened oscillation shows its way when the envelope settling time becomes longer than the oscillation period, such as at position C.

In Fig. 7, the simulated 0.1% settling time is plotted against different compensations. As we previously discussed,

Table 1. OPAMP1 Characteristics

DC-gain	88dB
Unity-gain freq.	725MHz
Load cap.	2pF
Phase margin	49°
Bias current	5.2mA
Output-swing	3V
Supply voltage	5V

there exists an optimal compensation to achieve the best settling. For OPAMP1, the shortest 0.1% settling time is 4.5ns, and it is achieved when $C_{cgb} = 700fF$. As we can see in Fig. 7, the compensation capacitance window needed to achieve a short settling time is wide, which makes the compensation-based settling optimization method robust for fabrication variations.

5. CONCLUSION

A design methodology for a gain-boosted OPAMP is presented. The settling performance of the gain-boosted OPAMP will be subject to two potential problems: the presence of the doublet and instability, which involves the pole-zero evolution shown in Fig. 7. The methodology enables designers to strike a balance between the two problems so as to achieve optimal OPAMP design in terms of settling performance.

A sample telescopic gain-boosted OPAMP is designed using this methodology. The exact characteristics are shown in Table 1. The sample/hold front-end in Fig. 3 using OPAMP1 can achieve an SNR of 78dB with an input signal of 8.1MHz in frequency and $2V_{p-p}$ in amplitude.

6. REFERENCES

[1] D. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, New York, 1997

[2] K. Bult and G. Geelen, "A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain", *IEEE J. Solid-State Circuit*, vol. 25, pp.1379-1384, Dec., 1990

[3] B.J. Hosticka, "Improvement of the Gain MOS Amplifiers", *IEEE J. Solid-State Circuits*, vol. 14, pp. 1111-1114, Dec, 1979

[4] B.Y.Kamath and R.G.Meyer and P.R.Gray, "Relationship Between Frequency Response and Settling Time of Operational Amplifiers", *IEEE J. Solid-State Circuits*, vol. SC-9, pp.347-352, Dec. 1974

[5] D. Fandre and A. Viviani, "Improved Synthesis of Gain-Boosted Regulated Cascode CMOS Stages Using SymbolicAnalysis and gm/ID Methodology", *IEEE J. Solid-State Circuits*, vol. 32, pp. 1006-1012, Jul. 1997

[6] M. Das, "Improved Design Criteria of Gain-Boosted CMOS OTA with High-Speed Optimizations", *IEEE Trans. on Circuits and Systems II*, vol. 49, pp. 294-297, Mar. 2002